

FIG. 2



US-PAT-NO: 6366524

DOCUMENT-IDENTIFIER: US 6366524 B1

TITLE: Address decoding in
multiple-bank memory architectures

----- KWIC -----

Abstract Text - ABTX (1):

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time, it is available to direct the

United States Patent
Abdifard

(10) Patent No.: US 6,366,524 B1
(45) Date of Patent: Apr. 2, 2002

ADDRESS DECODING IN MULTIPLE-BANK
MEMORY ARCHITECTURESInventor: Ebrahim Abdifard, Sunnyvale, CA
(US)Assignee: Micron Technology Inc., Boise, ID
(US)

Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

App. No.: 08/618,197

Filed: Jan. 24, 2000

Int. Cl. G11C 8/00

U.S. Cl. 365/230.06; 365/230.03; 365/230.08

Field of Search 365/230.06, 230.03, 365/230.06, 185.11

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Primary Examiner—Huan Hoang
(74) Attorney, Agent, or Firm—Fogg Silver Polglaze Lebert & Jay, P.A.

(57) ABSTRACT

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time, it is available to direct the second portion of the address to a proper decoder substantially without delay.

46 Claims, 8 Drawing Sheets

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FAST [1 wsp 1]

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☐ L8: (19) 7 and address
☐ L9: (5) 8 not 5
☐ L10: (46) 2 and address
☐ L12: (52) 10 or 11
☐ L13: (13) 12 and more
☐ L11: (15) 2 and address

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6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6215709 B1	20010410	89	Synchronous dynamic random access memory device	365/189.11	365/189.09; 365/194;	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6212111 B1	20010403	89	Synchronous dynamic random access memory device	365/200	365/189.07	
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6172935 B1	20010109	90	Synchronous dynamic random access memory device	365/233	365/194; 365/230.08	
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10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6005592 A	19991221		Image processing apparatus having improved memory	345/571	345/531	
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5953738 A	19990914	22	DRAM with integral SRAM and arithmetic-logic units	711/105	711/114; 711/5	
12	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5808948 A	19980915	9	Semiconductor memory device	365/201	365/200; 365/230.03	
13	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5761694 A	19980602		Multi-bank memory system and method having addresses	711/5	365/230.03; 365/230.06;	
14	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5313624 A	19940517		DRAM multiplexer	714/6	714/763	
15	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4473877 A	19840925		Parasitic memory expansion for computers	711/2		

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☒ L9: (5) 8 not 5
☒ L10: (46) 2 and add
☒ L12: (52) 10 or 11
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1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010050860 A1	20011213	37	Non-volatile memory with background operation	365/185.11		
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6373752 B1	20020416	88	Synchronous dynamic random access memory device	365/189.05	365/189.11; 365/230.06;	
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6351404 B1	20020226	88	Synchronous dynamic random access memory device	365/51	365/63	
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6333889 B1	20011225		Logic-merged semiconductor memory having high internal	365/230.03	365/51; 365/63;	
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6215726 B1	20010410	23	Semiconductor device with internal clock generating	365/233	327/141; 327/155;	
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8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6172935 B1	20010109	90	Synchronous dynamic random access memory device	365/233	365/194; 365/230.08	
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6125432 A	20000926		Image process apparatus having a storage device with	711/157	345/545; 345/572;	
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6005592 A	19991221		Image processing apparatus having improved memory	345/571	345/531	
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5953738 A	19990914	22	DRAM with integral SRAM and arithmetic-logic units	711/105	711/114; 711/5	

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rows in all of the banks 20 within the SDRAM 10. Examples of other well known commands include, but are not limited to, the ACTIVE, READ, WRITE, BURST TERMINATE, AUTO REFRESH, LOAD MODE REGISTER, COMMAND INHIBIT and NOP commands.

(13) The ACTIVE command is used to open up (or activate) a row of memory cells in a particular bank 20 for a subsequent access. The row remains active until a PRECHARGE command deactivates it. The READ command is used to initiate a burst read access for an active row. The WRITE command is used to initiate a burst write access for an active row. The READ and WRITE commands will also be accompanied with the column and bank addresses to complete the addressing for the command. The AUTO REFRESH command is used to refresh the contents of the memory arrays 20. The BURST TERMINATE command is used to truncate a read burst. The LOAD MODE REGISTER allows a mode register of the control circuit 12 to be loaded. The mode register contains information such as burst length and

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Schaefer

(45) Date of Patent: *Aug. 29, 2000

[54] SYNCHRONOUS DRAM MEMORY WITH ASYNCHRONOUS COLUMN DECODE

1745 [unclear] Scott Schuster, Born, 13.

73) **Amalgam Microtechnology, Inc., Boise, Id.**

* Notice: This patent is subject to a terminal disclaimer.

*1:2 ATT. No: 02318.00

21 FEB 1959

Related U.S. Applications Data

63. Continuation of application No. 39,534,464, Sep. 12, 1987
which is a continuation of application No. 06,772,874, Dec.
23, 1984, Pat. No. 4,731,654, which is a continuation of
application No. 39,522,669, Sep. 1, 1985, Pat. No. 4,600

11. IN C. G1C 400

U.S. CL. to Bureau of the Census 164232, 36523

Field of Search: 154-233.5, 23, 24, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855,

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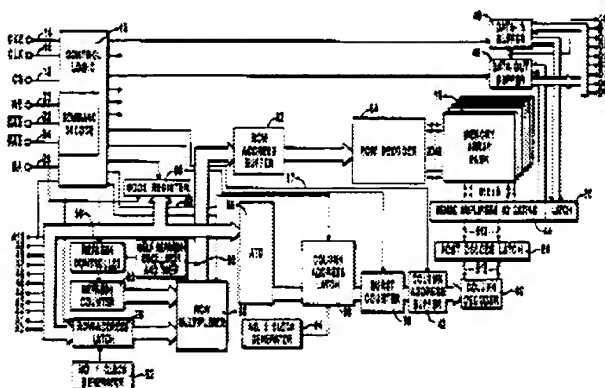
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ABSTRACT

ABSTRACT

Described is a synchronous DRAM memory model with control circuitry that allows the memory module to operate in burst mode. In burst mode, the address is obtained from the external address bus and the data is obtained from the external address bus immediately after a new address is present on the address bus. It uses an on-chip waiting for the column-address strobe signal to synchronize with the rising or falling edge of the asynchronous clock signal. Also described is a manner of connecting the memory circuitry which states that new column-addresses may be decoded and held within a buffer and the column-address strobe signal contains the circuitry that the column-addresses are correct and it is to be input into the microprocessor. Thus, each new column-address will be decoded immediately after it is present on the address bus and subsequent column-addresses will be discarded, while stored on-chip-addresses are input into the memory array. This results only upon the presence of the column address strobe which decodes the column address is held. The present invention improves the access rates of read and write operations in asynchronous DRAM memory by up to a complete clock cycle.

46 Claims, 6 Drawing Sheets





[75] Inventor: Yoshioaki Okajima, Kawasaki, Japan
 [75] Assignee: Fujitsu Limited, Kawasaki, Japan
 (*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(c), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

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Primary Examiner—Eddie F. Chan
 Assistant Examiner—Kimberly McLean
 Attorney, Agent, or Firm—Nakido, Maruchstein, Murray & Ortiz LLP

[21] Appl. No: 08/792,134
 [22] Filed: Jan. 31, 1997
 [30] Foreign Application Priority Data
 Feb. 2, 1996 [JP] Japan 8-017990
 [51] Int. Cl. G06F 12/00
 [52] U.S. Cl. 711/169; 711/5; 711/68; 711/167
 [56] Field of Search 711/4, 5, 105, 711/166, 111, 147, 148, 149, 150, 151, 152, 167, 168, 170, 173

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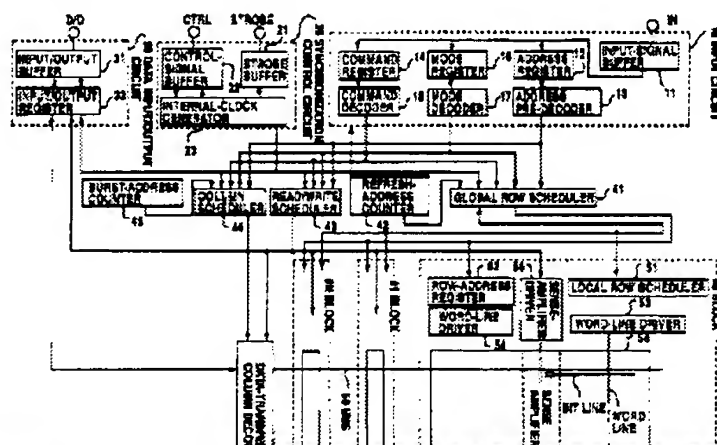
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ABSTRACT

A memory system using at least one DRAM chip and equipped with an interface for transferring input/output data in a packet format includes a plurality of banks within each of the at least one DRAM chip. The memory system further includes a control circuit for accessing a bank for data transfer of a given packet when the bank is different from a previous bank accessed for an immediately preceding packet, and for waiting for an operation to complete in the bank when the bank is the same as the previous bank.

6 Claims, 17 Drawing Sheets



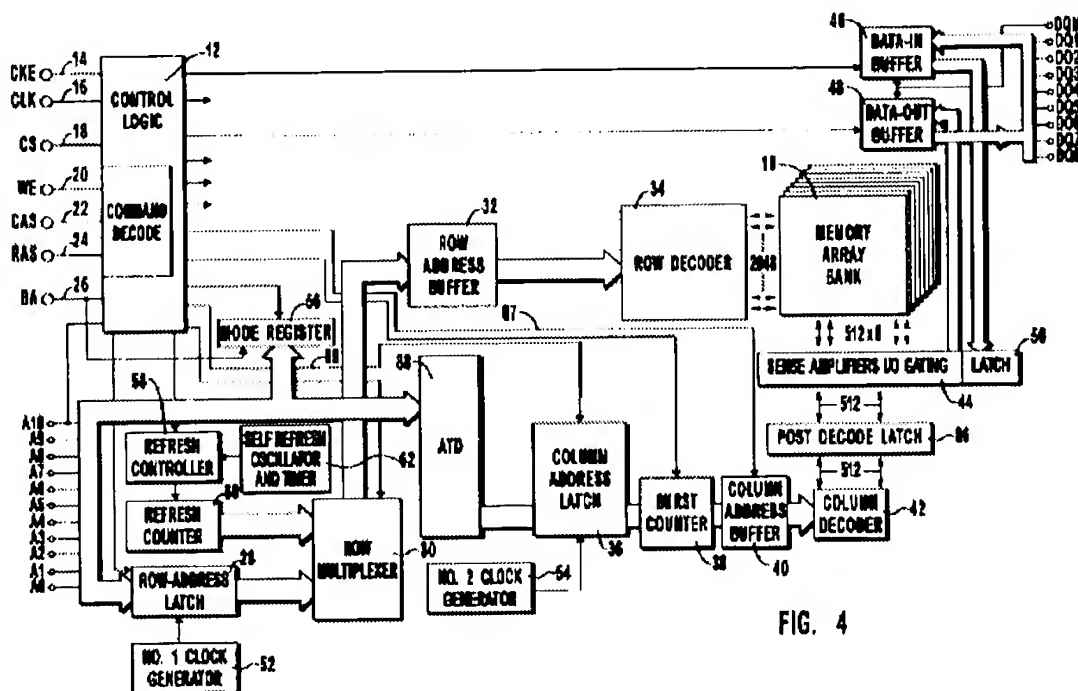


FIG. 4

U.S. Patent

Jun. 15, 1999

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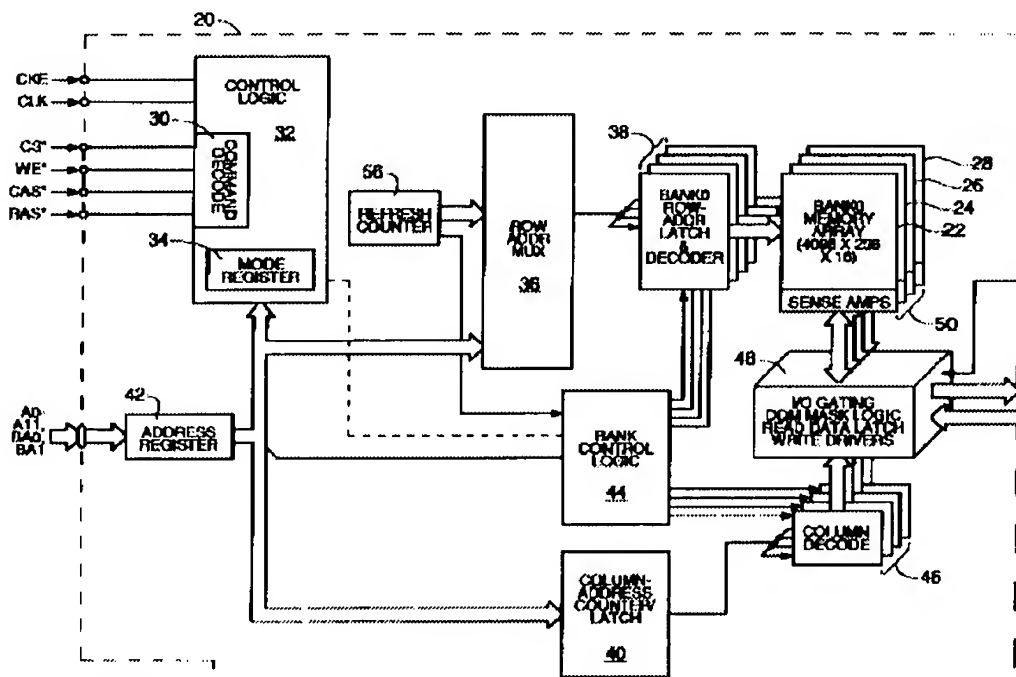


FIG. 1A

FIGURE 1B

U.S. Patent

Aug. 21, 2001

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